REMARKS

Initially, Applicants would like to express their appreciation of the courtesy extended by the Examiner in conducting a personal interview on August 3, 2001. During the interview, the novelty and benefits of the present invention embodied in Claims 62-65 as amended above and new Claims 66-79 were discussed.

If there are any questions with regards to this preliminary amendment, the undersigned attorney can be contacted at the listed telephone number.

Respectfully submitted,

PRICE AND GESS

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims have been amended as follows:

62. (Amended) A data processor performing data processing based on an 8-bit instruction, comprising:

a plurality of registers;

a decoding unit decoding an 8-bit instruction, the instruction independently designating:

one of a plurality of operations including transfer and calculation;

one of the plurality of registers as a source operand, and

one of the plurality of registers as a destination operand;

wherein [the plurality of registers includes at least one register] at least one of the source operand register and the destination operand register is capable of storing an address exceeding 16 bits; and

an execution unit for executing the decoded instruction.

63. (Amended) A data processor performing data processing based on an 8-bit instruction, comprising:

a plurality of registers;

a decoding unit decoding an 8-bit instruction, the instruction independently designating:

one of a plurality of operations including transfer and calculation;

one of the plurality of registers as a source operand, and

one of the plurality of registers as a destination operand;

wherein at least one instruction is further followed by a [numeric code] linear absolute address of more than 16 bits; and

an execution unit for executing the decoded instruction.

64. (Amended) A data processor performing data processing based on an 8-bit instruction, [the instruction independently designating:

one of a plurality of operations including transfer and calculation;

one of a plurality of registers as a source operand, and

one of the plurality of registers as a destination operand;

wherein a first register and a second register are included in the plurality of registers, and

a judgement of which one of sign-extending and zero-extending is to be performed on operand data is made depending on which of the first register and the second register is designated as the destination operand in the instruction] comprising:

a first register and a second register,

a decoding unit decoding an 8-bit instruction,

a judgment means for judging which one of sign-extending and zero-extending is to be performed on operand data is made depending on which of the first register and the second register is designated as the destination operand in the instruction, and

an execution unit for executing the decoded instruction.

65. (Amended) A data processor performing data processing based on an 8-bit instruction, comprising:

a plurality of registers;

a decoding unit for decoding an 8-bit instruction, the instruction independently designating:

one of a plurality of operations including transfer and calculation;

one of the plurality of registers as a source operand, and

one of the plurality of registers as a destination operand;

wherein an address register and a data register are included in the plurality of registers, and

an address stored in the address register is longer than data stored in the data register.

New Claims 66-79 are submitted for examination on their merits.